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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,000	01/13/2004	Kevin P. Grundy	SIPI.P117	4885

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EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,000	GRUNDY ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) *44-77* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,19,20,26,27,30-33 and 38* is/are rejected.

7)☒ Claim(s) *6-18,21-25,28,29,34-37 and 39-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/28/06 ; 02/04/06 ; 12/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 44-77 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on September 11, 2006 responding to Election/restriction requirement dated July 12, 2006.

2. Claims 1-43 are therefore pending in the application under prosecution.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 19-20, 26-27, 30-33, 38, are rejected under 35 U.S.C. 102(b) as being anticipated by US 2002/0083255 (Greeff et al).

With respect to claims 1-5, 19-20, 26-27, 30-33, and 38, Greeff teaches the invention as claimed:

a plurality of memory devices coupled one to another in a chain *(Fig. 1 shows a plurality of memory devices connected in a chain)*;

a memory controller coupled to the chain and configured to output a memory access command that is received by each of the memory devices in the chain and that selects a set of two or more of the memory devices to be accessed *(Fig. 1 shows a memory controller connected to the memory chain to select the memory devices to be accessed, the memory devices consisting of a set of two or more memory devices [See Fig. 1 and corresponding text in paragraph 0031-0032]*;

memory access command being a memory read command that selects a set of the memory devices to be read by the memory controller *(memory controller 31 and memory modules 24-26 connected in a point-to-point data connection during read/write operations) [Paragraph 0037]*;

memory access command being memory write command that selects a set of the memory devices to store a sequence of write data values *(memory controller 31 and memory modules 24-26 connected in a point-to-point data connection during read/write operations) [Paragraph 0037]*;

the set of memory device comprising fewer than all the memory devices in the chain *(memory controller 31 and memory modules 24-26 connected in a point-to-point data connection and memory modules 24, 26 connected in a daisy-chain fashion) [Paragraph 0036]*;;

each of the memory devices in the chain, except a last memory device, comprises an output port coupled to an input port of another of the memory devices *[memory modules 24-26 connected in a point-to-point data connection forming a daisy-chain connection) [Paragraph 0036-0037]*;

a first memory device in the chain comprising an input port coupled to the memory controller to receive the access command *[memory modules 24-26 connected in a point-to-point data connection forming a daisy-chain connection, the first memory to receive access commands) [Fig. 1; Paragraph 0036-0037]*;

each of the plurality of memory devices being a discrete integrated circuit device, a portion being mounted on the substrate [Fig. 1, Paragraph 0031-0032].

5. Claims 1-5, 19-20, 26-27, 30-33, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by US 2004/0030803 (Eatherton et al).

With respect to claims 1-5, 19-20, 26-27, 30-33, and 38, Eatherton teaches the invention as claimed:

a plurality of memory devices coupled one to another in a chain *(Fig. 1C shows a plurality of memory devices connected in a chain)*;

a memory controller coupled to the chain and configured to output a memory access command that is received by each of the memory devices in the chain and that selects a set of two or more of the memory devices to be accessed *(Fig. 1B-1C shows a memory controller connected to the memory chain to select the memory devices to be*

accessed, the memory devices consisting of a set of two or more memory devices [See Fig. 1 and corresponding text in paragraph 0030-0031];

memory access command being a memory read command that selects a set of the memory devices to be read by the memory controller *(control logic/processing element 150 and memory modules / associative memories 156, 158 connected in a point-to-point data connection during read/write operations) [Paragraph 0031]*;

memory access command being memory write command that selects a set of the memory devices to store a sequence of write data values *(control logic/processing element 150 and memory modules / associative memories 156, 158 connected in a point-to-point data connection during read/write operations) [Paragraph 0031]*;

the set of memory device comprising fewer than all the memory devices in the chain *(control logic/processing element 150 and memory modules / associative memories 156, 158 connected in a point-to-point data connection during read/write operations) [Paragraph 0031]*;

each of the memory devices in the chain, except a last memory device, comprises an output port coupled to an input port of another of the memory devices *(control logic/processing element 150 and memory modules / associative memories 156, 158 connected in a point-to-point data connection during read/write operations) [Paragraph 0031]*;

a first memory device in the chain comprising an input port coupled to the memory controller to receive the access command *[memory modules / associative*

memories 156, 158 connected in a point-to-point data connection during read/write operations) [Fig. 1C];

each of the plurality of memory devices being a discrete integrated circuit device, a portion being mounted on the substrate [Fig. 1C, Paragraph 0034].

Allowable Subject Matter

6. Claims 6-18, 21-25, 28-29, 34-37, and 39-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

November 27, 2006